What is claimed is:

1. A semiconductor device comprising:

an analog reference signal;

a comparator function communicatively coupled to the reference signal;

a control function communicatively coupled to the comparator function;

a primary DAC function communicatively coupled to the state machine function and to a summing function;

a supplemental DAC function communicatively coupled to the state machine function and to the summing function; and

a target component communicatively coupled to the summing function and the comparator.

2. The device of claim 1, wherein the analog reference signal comprises a bandgap voltage.

3. The device of claim 1, wherein the analog reference signal comprises a clock signal.

4. The device of claim 1, wherein the comparator function comprises an independent device.

5. The device of claim 1, wherein the comparator function comprises a sub-portion of another device.

6. The device of claim 1, wherein the comparator function comprises a combination of hardware and software.

7. The device of claim 1, wherein the control function comprises a state machine function.

8. The device of claim 1, wherein the control function comprises a programmable logic device.

9. The device of claim 1, wherein the control function comprises a code segment operating on a processor.

10. The device of claim 1, wherein the primary DAC function comprises an independent DAC device.

11. The device of claim 1, wherein the primary DAC function comprises a sub-portion of a DAC device.

12. The device of claim 1, wherein the primary DAC function comprises a code segment operating on a processor.

13. The device of claim 1, wherein the supplemental DAC function comprises an independent DAC device.

14. The device of claim 1, wherein the supplemental DAC function comprises a sub-portion of a DAC device.

15. The device of claim 1, wherein the supplemental DAC function comprises a code segment operating on a processor.

16. The device of claim 1, wherein the summing function comprises an independent device.

17. The device of claim 1, wherein the summing function comprises a sub-portion of another device.

18. The device of claim 1, wherein the summing function comprises a code segment operating on a processor.

19. The device of claim 1, wherein the target component comprises a programmable array.

20. The device of claim 19, wherein the target component comprises a programmable resistor array.

21. The device of claim 19, wherein the target component comprises a programmable capacitor array.

22. The device of claim 19, wherein the target component comprises a programmable inductor array.

23. A method of providing high-resolution calibration of a programmable semiconductor component, the method comprising the steps of:

providing a programmable semiconductor component;

providing a goal value for the programmable semiconductor component;

providing primary and supplemental DAC functions;

providing a control function;

utilizing the control function to determine a first bit step of the primary DAC function corresponding to the goal value;

utilizing the control function to determine a second bit step of the supplemental DAC function corresponding to the goal value; and

combining bit codes of the first and second bit steps to provide a control word for programming the programmable semiconductor component.

24. The method of claim 23, further comprising the steps of:

providing a reference signal;

determining a differential between the reference signal and a programmed value of the programmable semiconductor component; and

communicating the differential to the control function.

25. The method of claim 24, wherein the steps of determining a differential, communicating the differential, utilizing the control function, and combining bit codes to provide a control word are performed as part of an iterative process.

26. The method of claim 23, wherein a plurality of supplemental DAC function are provided and the control function is utilized to determine bits steps for each, sequentially.

27. The method of claim 23, wherein the control function utilizes a dichotomy algorithm.

28. The method of claim 23, wherein the control function utilizes an incremental parsing algorithm.